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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,418	01/24/2001	Simon C. Steely JR.	15311-2325	4792

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EXAMINER	
LANE, JOHN A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,418	STEELY ET AL.	
	Examiner	Art Unit	
	Jack A Lane	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 presented for examination.

2. The examiner requests, in response to this Office action, any documentation known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any documentation used to develop the disclosed/claimed subject matter and any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. Specifically, the examiner is looking for an invalidate message that includes bits (masks) that indicate a path to processors. This request does not require applicant to perform a search. Support for this request is derived from 37 C.F.R. 1.56 and 1.105, however, it is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies

subsequent to the first communication responding to this request and any information disclosures beyond the scope of this request are subject to the fee and certification requirements of 37 CFR section 1.97. **A response to this inquiry is required** under 37 C.F.R. 1.105.

In the event documentation (e.g. newly submitted/previously submitted on an IDS, incorporated by reference or "common knowledge" generally found in the background section but not a publication) is determined to qualify as prior art, a discussion of relevant passages, figs. etc. with respect to the claims must be provided. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential.

The examiner also requests, in response to this Office action, a showing of support for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s). in the specification and/or drawing figure(s). Here again this request is derived from 37 C.F.R. 1.105.

In the present disclosure, the background section identifies several prior art multiprocessor systems having cache coherency schemes. Several devices known in the prior art appear to correspond to elements in the presently claimed invention. For example, the presence bits (sectored), cache coherency directory, network routing tables,

home node and intermediate switch (group switch) appear to correspond to the claimed masks (or directory), switching devices and decoded information. Applicant must specifically consider this prior art when complying with the above request/1.105 requirement. Additionally, any prior publications corresponding to the background art is requested.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-17 are rejected under 35 U.S.C. § 102(a and/or b) as being anticipated by the admitted prior art found in the background section of the present specification.

The claimed "cache coherency mechanism" corresponds to the cache coherency mechanism discussed on page 3 of the present specification. The claimed "multiple processors" correspond to the plural processor system (e.g. SMP) discussed throughout the background. The claimed "copies of data of interest" correspond to the copies of data within the processors. The claimed "paths through various switching devices"

correspond the intermediate or group switches. The claimed function of "encoding information that is indicative of the paths into...masks" corresponds to the presence bits and/or directory entries. Applicant should note the directory entries include addresses of processors. The claimed "invalidate message that includes the masks" corresponds to the bits transmitted along with an invalidate message used to access routing tables. The bits could be the presence bits, address bits etc. The claimed function of "decoding the applicable masks and routing the invalidate message" corresponds to the function of accessing routing tables with information from the message to identify paths to processors.

The examiner believes all dependent claim features not specifically discussed above are expressly or inherently taught by the admitted prior art. The remaining dependent claim features, while part of the invention, appear to be readily available (known) to the computer/cache memory designer and their relevance not essential to the main invention found in the independent claim(s). Thus, a detailed discussion of the well known claim feature(s) is not warranted at this time. Support for this line of reasoning is derived from 37 C.F.R. 1.105. 37 C.F.R. 1.105 permitting "stipulations as to facts" or "whether a dependent claim element is known in the prior art based on the examiner having a reasonable basis for believing so."

In the event applicant disagrees with the characterization of certain dependent claim elements as being "expressly or inherently" taught by the reference, applicant must

specify exactly what claim elements are considered "novel" or "allowable" and why they are allowable (e.g. the claim feature is not suggested/taught in the art of record).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant should review the prior art not relied upon for its relevance to the instant claims.

Webb, Jr. et al. (6,751,721) teaches a broadcast invalidate scheme. Webb's invalidate scheme appears to be similar to the backgrounds discussion of multiple-processor groups, group switches, "sectored presence bits."

Koren (6,421,712) teaches a computer system broadcasting invalidation messages.

Any response to this action should be mailed to:

Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for Official communications intended for entry)

Or:

(703) 872-9306, (for Non-Official or draft communications, please label "Non-Official" or "DRAFT")

JACK A. LANE
PRIMARY EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack A. Lane whose telephone number is 571 272-4208. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571 272-4210.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272-2100

JACK A. LANE
PRIMARY EXAMINER